REMARKS/ARGUMENTS

In view of the following remarks, Applicant respectfully requests reconsideration and allowance of the subject application. The actions taken herein place the Application in condition for allowance and Applicant respectfully requests that they be entered. Claim 14 is amended. No claims are cancelled. This amendment is believed to be fully responsive to all issues raised in the 5/06/04 Office Action.

CLAIM REJECTIONS

§112

Claim 14 stands rejected under §112 second paragraph for containing the limitation "the host computer device" without sufficient antecedent basis. Claim 14 is amended to read "the host processor" which was the intended language and has antecedent basis in the first limitation of claim 14 as originally filed. Thus, this amendment corrects a simple editing mistake and is not related to patentability or the scope of the claim. Applicant respectfully requests that the §112 rejection of claim 14 be withdrawn.

§103

Claims 1-3, 9, 13-14, 17 and 20 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert").

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Claim 4 stands rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,659,718 to Osman (hereinafter "Osman").

Claims 5-8 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,659,718 to Osman (hereinafter "Osman") and further in view of US Patent No. 5,142,683 to Burkhardt (hereinafter "Burkhardt").

Claims 10-11 and 18-19 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,142,683 to Burkhardt (hereinafter "Burkhardt").

Claim 12 stands rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,142,683 to Burkhardt (hereinafter "Burkhardt") and further in view of US Patent No. 5,659,718 to Osman (hereinafter "Osman").

Claims 21-23 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,675,807 to Iswandhi (hereinafter "Iswandhi").

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Mori is the primary reference relied upon by the Office for these rejections. Mori teaches an information recording apparatus including a plurality of controlling units for recording data received from a host device on an information recording medium. Mori describes a disk array apparatus configured by a plurality of hard disks 100 and two array disk control apparatuses 1 and 1' that control these hard disks 100. The array disk control apparatuses 1 and 1' are connected to a host device (not shown) via their respective interfaces (not shown) and control writing of data sent from the host device in the hard disks 100. The control apparatuses 1 and 1' have the same configuration and are configured so as to communicate with each other and control data sent from the host device and stored in duplicate. (Mori, col. 6, lines 1-13).

The array disk apparatus 1 comprises a cache memory 11 to temporarily store data exchanged between the host device and hard disk 100, a hard disk interface control section 12 that control the interface between the hard disk 100 and cache memory 11, a parity generator 13 that generates parity data when data is newly stored in the hard disk 100, a parity generation disabling flag 14 and cross call controlling means 15. (Mori, col. 6, lines 14-21).

The cross call controlling means 15 controls communications for data duplication between the two array disk control apparatuses 1 and 1' and exchange of information between the array disk control apparatuses such as

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operations of the parity generation disabling flag 11. (Mori, col. 6, lines 33-37).

Mori thus teaches a system where a first array disk control apparatus is connected to a host device via a dedicated interface and a second array disk control apparatus is connected to a host device via a second dedicated interface. A separate and distinct cross call control means allows communication between the first and second controllers.

Claim 1 is directed to a data array system for providing a host computer device having a host bus redundant access to a data storage device and recites:

- an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and
- a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link.

The Office acknowledges that Mori does not disclose "the active controller and standby controller linked to the host bus whereby the host bus functions as an inter-controller-link". The Office then looks to Herbert for this limitation.

Herbert teaches a RAID subsystem which includes a single RAID controller 40 and a disk array 100. (Herbert, col. 7, line 63- col. 8 line 5). The

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RAID controller 40 includes a DMA controller 71 and a disk drive interface controller 90. The DMA controller 71 and the disk drive interface controller 90 have separate and distinct functions and are coupled within the RAID controller via a RAID controller internal bus 51. The DMA controller 71 transfers data from the host 10 to the local memory 80. Col 8 lines 65-67. In contrast the disk controller 90 retrieves data from the local memory and writes it to the disk array. Col. 10 lines 1-3.

The PCI Bus Bridge interfaces the host's PCI bus 30 to the RAID controller's internal bus 51. (Herbert, col. 8 lines 6-13). Herbert does not teach or suggest active and standby controllers linked to a host bus which functions as an inter-controller-link. As illustrated above, Herbert teaches a single RAID controller system which includes a DMA controller and a disk drive interface controller.

The Office continues that it would have been obvious to one of the skill in the art at the time of the present invention to combine the teachings of Mori and Herbert. Applicant respectfully disagrees for at least the following reasons.

The Office has failed to make out a §103 prima facie case for at least three reasons. First, the Office has provided no motivation to combine the references. Such motivation or suggestion must be found in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine the reference teachings. In the

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present instance the Office has not provided any suggestion or motivation from the references.

Instead, the Office relies solely on its conclusion that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the active controller and the standby controllers both linked directly to the host PCI bus as taught by Herbert in the system of Mori to minimize the number of buses for connecting devices and thus reduce the system cost". (Office Action pg. 3). As described above Applicant respectfully disagrees that Herbert teaches an "active controller and the standby controllers both linked directly to the host PCI bus". However, even hypothesizing arguendo that Herbert does teach such features, the Office fails to provide any evidence that such a system would be less costly. The systems of Mori, Herbert and the present application have multiple inter-related components. To assert, without supporting documentation, that substituting a given component in a system would make that system less expensive, is arbitrary and capricious and creates a record devoid of reviewable evidence. Applicant specifically requests that the Office provide evidence that the Office's change to Mori's system would decrease the costs of such a system.

Further, the Office is asserting that it would have been obvious to replace Mori's two interfaces for connecting the individual control apparatuses to the host device and the cross call controlling means 15 and 15' for communication between the two controllers with a link to the host bus which performs both functionalities in order to decrease costs. This assertion

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directly contradicts MPEP §2144.04 (II)(B) which states that "omission of an element with retention of the element's function is an indicia of **unobviousness**".

Not only has the Office provided no motivation to combine the references, it has not provided any explanation why one of skill in the art who wanted to modify Mori's multi-controller system would look to the single RAID controller system of Herbert. Presently, the record is devoid of any suggestion or motivation for one of skill in the art to combine the teachings of Mori and Herbert.

Second, the Office fails to establish a prima facie § 103 rejection, because the Office has not provided any evidence that combining Mori and Herbert would have a reasonable expectation of success. Mori teaches a system where a first array disk control apparatus is connected to a host device via a dedicated interface which is not shown or described and a second array disk control apparatus is connected to a host device via a dedicated interface which is not shown or described. A separate and distinct cross call control means allows communication between the first and second controllers. The record does not contain any evidence that combining the single RAID controller system of Herbert with Mori's system would be successful. Mori relies on a separate and distinct cross-calling controlling means for inter-controller communication. The art of record contains no evidence that such a combined system would allow the host bus to act as the inter-controller-link. As such the record is void of evidence that the proposed combination would

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have a reasonable expectation of success in creating a system comprising the limitations of claim 1.

Third, the Office fails to establish a prima facie § 103 rejection because the prior art references when combined do not teach or suggest all the claim limitations. Claim 1 recites the limitation that "the host bus functions as an inter-controller-link". The Office admits that Mori does not teach such a limitation. Further Herbert does not disclose or teach active and passive controllers linked to the host bus which also acts as an inter-controller-link. Both references lack the same limitation of claim 1 and as such the art of record does not teach all of the claim limitations of claim 1 which consequently cannot be rendered obvious by those references. For at least the reasons discussed above, Applicant respectfully requests the § 103 rejection of claim 1 be withdrawn.

Claims 2-8 depend from claim 1 and as such contain limitations not taught or suggested by the art of record. Therefore, Applicant respectfully requests the §103 rejection of claims 2-8 be withdrawn.

Claims 9-13 contain similar features to those of claim 1 which are not shown or suggested by the art of record. Applicant respectfully requests that the associated §103 rejection be withdrawn.

Claim 14 is directed to a data storage system with redundant data storage and recites:

- a host processor;

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- an active controller controlling access by the host processor to data storage devices;
- a standby controller controlling access by the host processor to the data storage devices; and
- a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus.

The Office acknowledges that Mori does not disclose "a host bus communicatively linking the host processor, the active controller, and the standby controller, to assert and sample signals on the host bus to provide inter-controller communications over the host bus". The Office then looks to Herbert for this limitation and states that "Herbert teaches redundant controllers that attach directly to the host system's main PCI bus". Applicant respectfully disagrees with the Office's characterization of Herbert's teachings. Herbert teaches a system which utilizes a single RAID controller. The single RAID controller includes a DMA controller 71 and a disk drive interface controller 90. The DMA controller and the disk drive interface controller have distinct functionalities. Herbert does not characterize these controllers as active and standby. In this regard Herbert is non-analogous art with Mori. Even hypothesizing arguendo that the Office's characterization of

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Herbert is correct, the Office still has not provided any suggestion or motivation from the references as to why one of skill in the art would have been motivated to combine their teachings. At least for these reasons claim 14 is allowable over the art of record.

Neither Mori nor Herbert nor a combination thereof teach or describe "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus" as recited in claim 14. At least for this additional reason Applicant respectfully requests that the §103 rejection of claim 14 be withdrawn.

Claims 15-20 depend from claim 14 and as such contain limitations not taught or suggested by the art of record. Therefore, Applicant respectfully requests the §103 rejection of claims 15-20 be withdrawn.

Claim 21 is directed to a method for providing inter-controller communications between an active controller and a standby controller configured for redundant communications between a host and a storage device and linked to a host bus, and recites:

- at the standby controller, specifying a range of memory in the standby controller as an interrupt range;
- with the active controller, writing data to the interrupt range of the standby controller; and
- at the standby controller, driving a local interrupt.

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The Office admits that Mori and Herbert do not teach the limitations of claim 21 namely, "writing data to the interrupt range of the standby controller; and at the standby controller, driving a local interrupt". The Office then looks to Iswandhi for these limitations. The Office states that it would have been obvious to combine these references. However, the Office does not provide any motivation or suggestion from the references for such a combination. Further, Iswandhi teaches directly away from the limitations of claim 21 in that it teaches a processing system composed of multiple sub-processing systems. Each sub-processing system has, as the main processing element, a central processing unit (CPU) that in turn comprises a pair of processors operating in lock-step, synchronized fashion to execute each instruction of an instruction stream at the same time. Col. 4 lines 44-50. In contrast, claim 21 is directed to an active controller and a standby controller performing distinct functions as evidenced from the limitations of claim 21, "at the standby controller, specifying a range of memory in the standby controller as an interrupt range", "with the active controller, writing data to the interrupt range of the standby controller", and "at the standby controller, driving a local interrupt".

The Office has failed to provide any motivation from the reference to combine the teachings of the art of record. Further, the art itself teaches away from such a combination. As such the Office has failed to establish a prima facia §103 rejection. Applicant respectfully requests that the §103 rejection of claim 23 be withdrawn.

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Claims 22-23 depend from claim 21 and as such contain limitations not taught or suggested by the art of record. Therefore, Applicant respectfully requests the §103 rejection of claims 22-23 be withdrawn.

Applicant notes that the §103 rejections of the pending claims combine multiple references without sufficiently identifying the motivation to combine such references. Applicant specifically requests that the Office's support for such combinations be entered into the record to further prosecution of the present application.

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Conclusion

Claims 1-23 are believed to be in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is encouraged to contact the undersigned attorney to discuss the unresolved issue.

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